NON-SYNCHRONIZED MULTIPLEX DATA TRANSPORT

ACROSS SYNCHRONOUS SYSTEMS

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10   ABSTRACT OF THE DISCLOSURE

A method allows two substantially asynchronous system components of a logic emulation system to exchange data packets with reference to a clock signal of predetermined frequency. In one example, each bit is transmitted across the system

15   components over two or more cycles of the clock signal. The reference clock signal can be distributed to the two system components from a common clock signal generator, or can be generated locally independently.

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